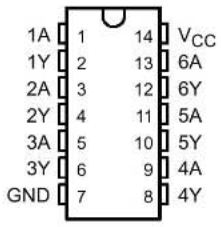
CS 2420 Lab 3

Topics: Logic and Delay in Chips

Pre Lab: Read through T4 and try to find the expected delay.

Warning: DO NOT GIVE THE CHIPS A VOLTAGE HIGHER THAN +5V

T1. Understand logic 0 in a digital circuit



Find the 7404 chip on the board. Connect pin Vcc to the "+5v" channel and the GND pin to "Ground". Connect pin 1A to the "Variable Power supply +" channel on the bottom left side of the board. Connect pin 1Y to LED 0.

Click and open the "Variable Supplies (**VPS**)" option on the NI Elvis instrument bar. You will see a knob for "Supply +" on the right side. Turn the knob to set the output voltage to 0. You should see LED 0 on, **because** (fill in reason below)

Increase the power ***slowly*** from 0V to 5V. At a voltage X_0, you should see the LED dim. Now, decrease the power slowly from 5V to 0V. At a voltage Y_0, you should see the LED fully on. Repeat increasing and decreasing the power a few times to find X_0 and Y_0 and fill in the table below.

Note that X_0 and Y_0 may not be the same. The minimum of X_0 and Y_0 is used as the threshold for logic 0, i.e. logic 0 means the voltage in the range of 0 to min(X_0, Y_0).

Change the Input	When Increasing	When Decreasing	Min(X_0, Y_0)
Threshold of 0	X_0 =	Y_0 =	

T2. Understanding logic 1 in a digital circuit

Repeat T1, but change the connections: connect pin 1A to the "Variable Power Supply +" channel, pin 1Y to pin 2A, and finally pin 2Y to LED 0.

Set the "Supply +" to 5V and you should see the LED 0 on **because** (fill in reason below)

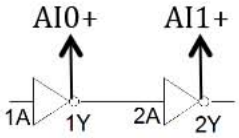
Decrease the power ***slowly*** from 5V to 0V. At a voltage Y_1 you should see the LED dim. Now, increase the power slowly from 0V to 5V. At a voltage X_1, you should see the LED fully on. Repeat decreasing and increasing the power a few times to find X_1 and Y_1 and fill in the table below.

Note that X_o and Y_o may not be the same. The maximum of X_1 and Y_1 is used as the threshold for logic 1, i.e. logic 1 means the voltage in the range of 1 to max(X_1, Y_1).

Change the Input	When Increasing	When Decreasing	Max(X_1, Y_1)
Threshold of 1	X_1 =	Y_1 =	

T3. Understand gate delay in a logic gate.

Still using the 7404 chip, make the connections necessary to create the figure on the right.



In this experiment, we use NI Elvis to generate a periodic 0-1 signal as input to the digital circuit and then probe outputs at pin 1Y and 2Y to measure the delay cause by the second inverter gate. So, connect pin 1A to the "Function Generator (FGEN)" channel on the left side of the board to get the input signal.
Connect pin 1Y to channel AI0+ and pin 2Y to AI1+ on the upper left side of the board. Finally connect channel AI0- and AI1- to the Ground channel.

Now click and open the "Function Generator (**FGEN**)" option from the instrument bar. Choose the "Rectangle" option for waveform type, 2.50V for the Amplitude and DC Offset settings. Click 100 kHz for the Frequency.

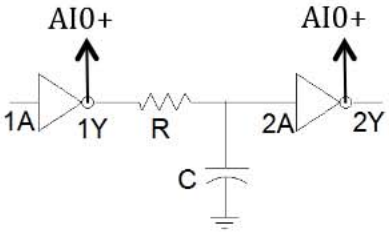
Now click and open the "Oscilloscope (**SCOPE**)" option from the instrument bar. For channel A, choose AI0+ for source, 2V/div for Scale, Zero for Position, and DC for coupling. For Channel B, choose AI1+ for source, 2v/div for Scale, Zero for Position, and Dc four Coupling. Then, set 5us/div for Time Base. Finally, make sure to turn on Channel A, Channel B, and cursor.

You should see a steady green curve and a steady blue curve on the oscilloscope, and some data at the bottom. The green curve shows the input to the second inverter gate. The blue curve shows the output from the second inverter gate. You should see that the blue curve is delayed with the green curve cause by the gate.

Explain what you should see if there is no delay in the gate.

Now, on the left side, find two dashed lines C1 and C2. Drag C1 to a down slope of the green curve and drag C2 to an up slope of the blue curve that is close to but behind C1. Read the data dT that shows the delay _____

T4. Understand propagation delay between two logic gates.



Propagation delay refers to the time for a signal to propagate from the output of a gate to the input of the next gate. Because gates are connected by wires, we can model the output of the first gate, the wire and the input of the second gate in the right figure: a resistor R and a capacitor C. The propagation delay is roughly the multiplication of R and C. For example, if R is 10Ω and C is 10pF, the delay is about 10Ω x 10pF = 100ps, which is NOT a small delay in high speed digital circuits nowadays. Note that the 74xx chips in our labs are NOT high speed logic gates.

To understand the propagation delay, we put a resistor of 1kΩ and a capacitor of 1μF between 1Y and 2A, so that the delay is amplified and observable by NI Elvis.

Now, connect other pins and channels as in T3 and turn on the Function Generator and Oscilloscope in NI Elvis. But, in the Function Generator, we click 100Hz for frequency and in the oscilloscope, we 2ms/div for Time Base. We can expect the delay to be _____ while the measured delay dT is _____.